AMENDMENTS TO THE CLAIMS:

Please cancel Claims 1 through 22 and add the following new Claims 23 through 44.

23. (New) A host processor to camera interface, comprising:

a camera side interface, including:

a camera side link layer coupled to a camera, the camera providing video data, the camera side link layer converting the video data to a desired video data format;

a serializer coupled to the camera side link layer for serializing the video data in the desired video data format; and

a camera side transmitter coupled to the serializer, the camera side transmitter transmitting the serialized video data;

a host processor side interface, including:

a host processor side receiver for receiving the serialized video data;

a deserializer coupled to the host processor side receiver, the deserializer deserializing the serialized video data; and

a host processor side link layer coupled to the deserializer and a host processor, wherein the host processor side link layer is adapted to convert the deserialized video data into a format compatible with the host processor when required; and

a cable for carrying the video data, the cable including a pair of power wires for carrying power, the cable coupling the camera side transmitter to the host processor side receiver.

24. (New) The interface of claim 23, wherein the camera side link layer is configured to convert a plurality of camera video data formats into the desired video data format.

25. (New) The interface of claim 24, wherein the camera video data formats include a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format.

26. (New) The interface of claim 24, wherein at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal, and wherein the camera side link layer combines the FVAL signal and the LVAL signal into a single validation (XVAL) signal that is provided to the host processor side link layer.

27. (New) The interface of claim 26, wherein the XVAL signal corresponds to the LVAL signal with an added end-of-frame (EOF) signal.

28. (New) The interface of claim 27, wherein a pulse width of the EOF signal is less than a pulse width of the LVAL signal.

29. (New) The interface of claim 23, wherein the functionality of the host processor side link layer is incorporated within the host processor.

30. (New) The interface of claim 23, further including:

a low-voltage differential signaling (LVDS) receiver for serial-to-camera (SERTC) channel communications located within the camera side interface, wherein inputs of the LVDS receiver are coupled to outputs of the camera side transmitter and an output of the LVDS receiver is coupled to the camera side link layer; and

an LVDS transmitter for SERTC channel communications located within the host processor side interface, wherein the SERTC channel is provided for reconfiguring the camera, and wherein an input of the LVDS

transmitter is coupled to the host processor side link layer and outputs of the LVDS transmitter are coupled to inputs of the host processor side receiver.

31. (New) The interface of claim 30, wherein the cable includes a first pair of signal wires for carrying the video data, and wherein the video data is in the form of a low-voltage differential signaling (LVDS) data stream.

32. (New) The interface of claim 31, wherein the camera side link layer and the host processor side link layer are configured to share the first pair of signal wires to communicate the video data in the desired video signal format and configuration signals for the SERTC channel.

33. (New) The interface of claim 30, wherein the cable further includes:

a second pair of signal wires to communicate configuration signals for the SERTC channel.

34. (New) A host processor to camera interface for a motor vehicle, comprising:

a camera side interface, including:

a camera side link layer coupled to a camera, the camera providing video data, the camera side link layer converting the video data to a desired video data format, wherein the camera is attached to the motor vehicle;

a serializer coupled to the camera side link layer for serializing the video data in the desired video data format; and

a camera side transmitter coupled to the serializer, the camera side transmitter transmitting the serialized video data;

a host processor side interface, including:

a host processor side receiver for receiving the serialized video data;

a deserializer coupled to the host processor side receiver, the deserializer deserializing the serialized video data; and

a host processor side link layer coupled to the deserializer and a host processor, wherein the host processor side link layer is adapted to convert the deserialized video data into a format compatible with the host processor when required, and wherein the host processor is incorporated within an electronic control unit (ECU) of the motor vehicle that is remote from the camera; and

a cable for carrying the video data, the cable including a pair of power wires for carrying power, the cable coupling the camera side transmitter to the host processor side receiver, wherein the camera side link layer is configured to convert a plurality of camera video data formats into the desired video data format, and wherein the camera video data formats include a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format.

35. (New) The interface of claim 34, wherein at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal, and wherein the camera side link layer combines the FVAL signal and the LVAL signal into a single validation (XVAL) signal that is provided to the host processor side link layer.

36. (New) The interface of claim 35, wherein the XVAL signal corresponds to the LVAL signal with an added end-of-frame (EOF) signal.

37. (New) The interface of claim 36, wherein a pulse width of the EOF signal is less than a pulse width of the LVAL signal.

38. (New) The interface of claim 34, wherein the functionality of the host processor side link layer is incorporated within the host processor.

39. (New) The interface of claim 34, further including:

a low-voltage differential signaling (LVDS) receiver for serial-to-camera (SERTC) channel communications located within the camera side interface, wherein inputs of the LVDS receiver are coupled to outputs of the camera side transmitter and an output of the LVDS receiver is coupled to the camera side link layer; and

an LVDS transmitter for SERTC channel communications located within the host processor side interface, wherein the SERTC channel is provided for reconfiguring the camera, and wherein an input of the LVDS transmitter is coupled to the host processor side link layer and outputs of the LVDS transmitter are coupled to inputs of the host processor side receiver.

40. (New) The interface of claim 39, wherein the cable includes a first pair of signal wires for carrying the video data, and wherein the video data is in the form of a low-voltage differential signaling (LVDS) data stream.

41. (New) The interface of claim 40, wherein the camera side link layer and the host processor side link layer are configured to share the first pair of signal wires to communicate the video data in the desired video signal format and configuration signals for the SERTC channel.

42. (New) The interface of claim 40, wherein the cable further includes:

a second pair of signal wires to communicate configuration signals for the SERTC channel.

43. (New) A method for sharing a pair of signal wires, comprising the steps of:

providing a trigger pulse from a host processor side link layer to a camera side link layer through a power line;

disabling a serializer in the camera side link layer and enabling a serial-to-camera (SERTC) channel receiver in the camera side link layer in response to receiving the trigger pulse on the power line;

monitoring the status of the pair of signal lines by examining outputs of a deserializer located in the host processor side link layer;

enabling a SERTC channel transmitter located in the host processor side link layer to establish a serial communication interface (SCI) between a camera coupled to the camera side link layer and a host processor coupled to the host processor side link layer via the pair of signal lines when the outputs of the deserializer indicate the pair of signal lines are free.

44. (New) The method of claim 43, further including the steps of:

disabling the SERTC channel transmitter and the SERTC channel receiver and enabling the deserializer and the serializer in response to a reset message, wherein the reset message is provided by the host processor sending a reset signal to the host processor side link layer.